

Fig. 1

Bus with multiple masters (and slaves):-

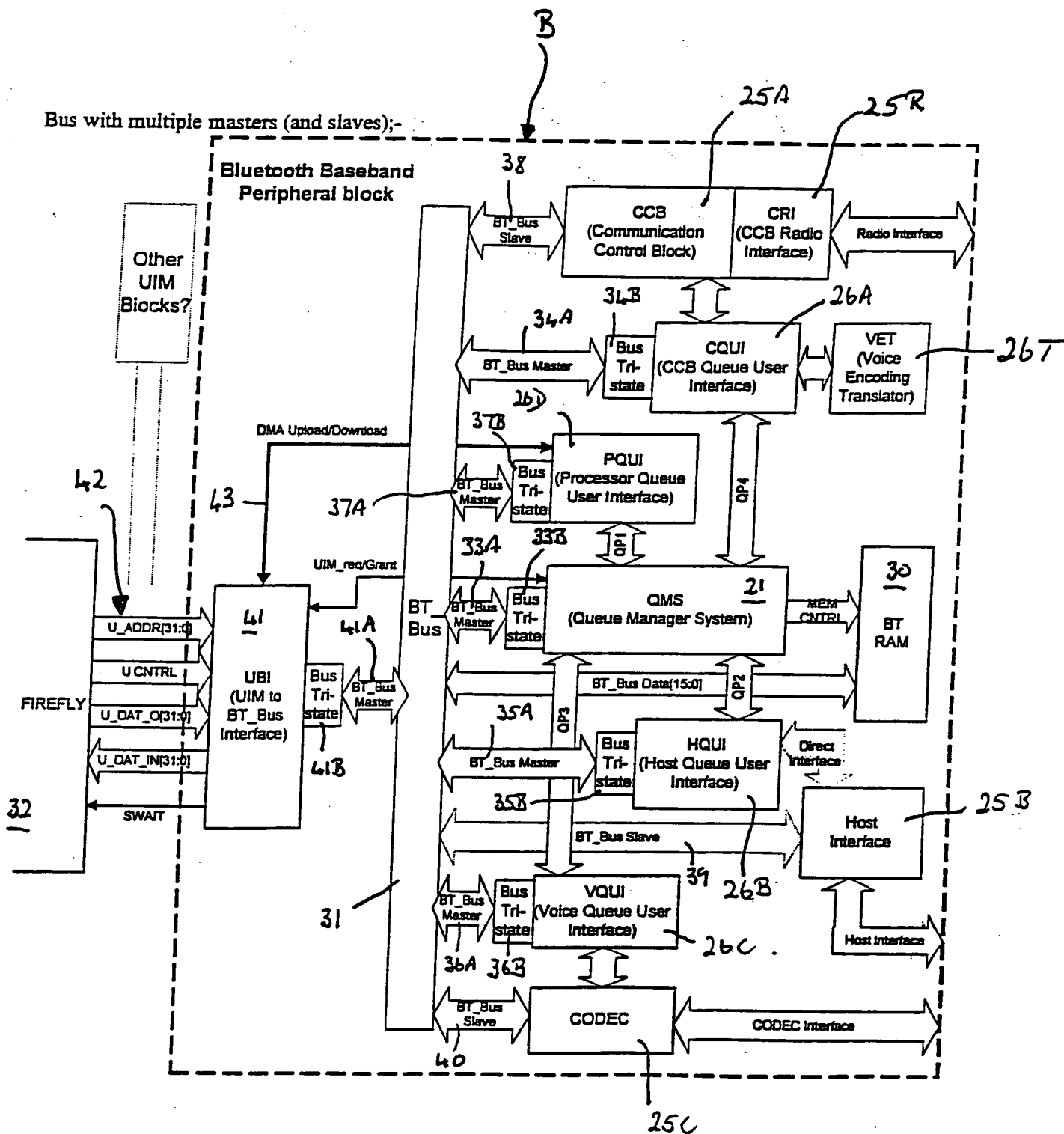


Fig. 2

Arbiter state machine;

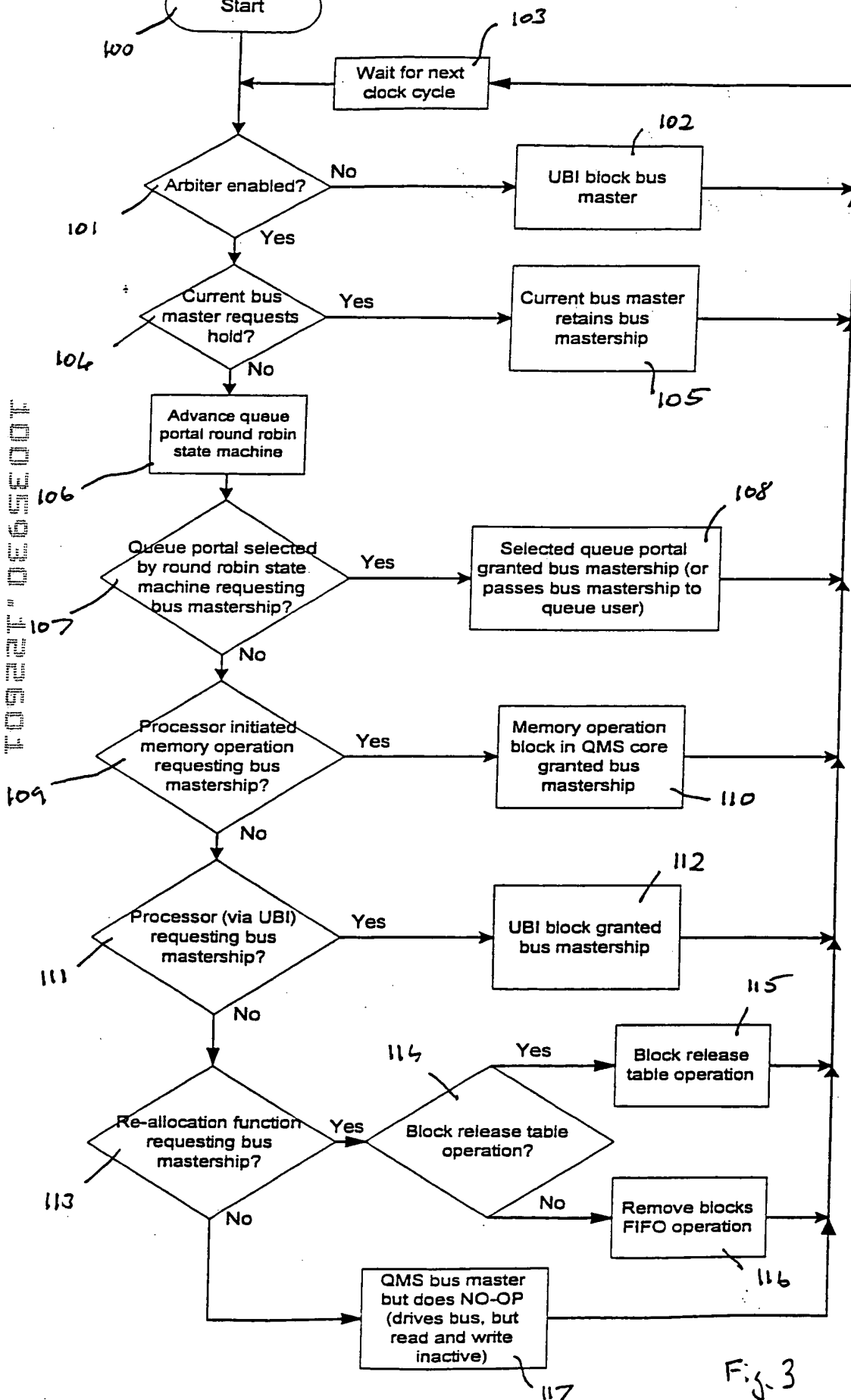


Fig. 3